# Getting Started with FPGA Advantage Tutorial

Software Version 5.1

7 August 2001

Contractor/manufacturer is:
Mentor Graphics Corporation
8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.

Web site: http://www.fpga-advantage.com
Email: FPGA_support@mentor.com

# Trademark Information

The following names which appear in this documentation set are trademarks, registered trademarks or service marks of Mentor Graphics Corporation:

HDL Designer Series™, HDL Designer™, HDL Pilot™, HDL Detective™, HDL Author™, HDL2Graphics™, FPGA Advantage™, Interconnect Table™, Interface-Based Design™, IBD™, Inventra™, LeonardoInsight™, LeonardoSpectrum™, Mentor™, Mentor Graphics®, Model*Sim*®, ModuleWare™, Renoir™, Seamless®, Seamless CVE™ and SpeedGate™.

The following names which appear in this documentation set are trademarks, registered trademarks or service marks of other companies:

Adobe, the Adobe logo, Acrobat, the Acrobat logo, Exchange, FrameMaker and PostScript are registered trademarks of Adobe Systems Incorporated.

Altera, APEX, MegaWizard and MAX+PLUS are registered trademarks and Quartus a trademark of Altera Corporation.

ClearCase Attache is a trademark and ClearCase is a registered trademark of Rational Software Corporation.

DesignSync is a registered trademark of Synchronicity Incorporated.

FLEXlm is a trademark of Globetrotter Software, Incorporated.

Hewlett-Packard (HP), HP-UX and PA-RISC are registered trademarks of Hewlett-Packard Company.

Leapfrog, NC-Verilog, Verilog and Verilog-XL are trademarks and registered trademarks of Cadence Design Systems Incorporated.

Netscape is a trademark of Netscape Communications Corporation.

SPARC is a registered trademark and SPARCstation is a trademark of SPARC International Incorporated.

SpyGlass is a trademark of Interra Inc.

Sun Microsystems and Sun Workstation are registered trademarks of Sun Microsystems Incorporated. Sun and SunOS are trademarks of Sun Microsystems Incorporated.

Synopsys, Design Analyzer, Design Compiler, FPGA Express, VCS, VCSi and VSS are trademarks of Synopsys Incorporated.

# TABLE OF CONTENTS

# About This Manual

This manual is a printable Acrobat PDF version of the online HTML *Getting Started with FPGA Advantage Tutorial*. It is provided for those users who prefer to work from a printed document.

The screen shots and path name convention (/) are the same as those used in the Windows environment. Some screen shots in the UNIX environment will look different from the ones shown in this tutorial. However, the design flow is the same for any configuration on all platforms.

# Getting Started with FPGA Advantage

## Welcome to FPGA Advantage

This simple tutorial presents the complete design flow for a sample design from HDL text import using, HDL2Graphics, HDL generation, simulation through to synthesis in approximately 30 minutes.

You should have installed at least one configuration of FPGA Advantage and obtained your evaluation or permanent licenses before starting this tutorial. Temporary evaluation licences can be obtained for *FPGA Advantage* or *FPGA Advantage Personal* from the FPGA Advantage website.

The Getting Started tutorial is based on HDL code recovered using HDL2Graphics and can be completed for VHDL or Verilog using any of the *FPGA Advantage Pro* or *FPGA Advantage Personal Pro* configurations.

A number of HDL Designer Series tutorials can also be run. See the Start Here Guide for more information.

# Invoking FPGA Advantage

You can invoke your installed configuration of FPGA Advantage on Windows by using the shortcut which was created by the install program on your desktop. Alternatively, you can choose the shortcut of your choice from the **FPGA Advantage 5.1** or **FPGA Advantage Personal 5.1** cascade of the **Programs** menu. One or more of the following options can be accessed from the Windows **Start** button if they are selected during installation.

```
FPGAdv Text       (for FPGA Advantage Text)
FPGAdv Graphics   (for FPGA Advantage Graphics)
FPGAdv Pro        (for FPGA Advantage Pro)


FPGAdv Personal Text     FPGAdv Personal Simulation Text
FPGAdv Personal Graphics FPGAdv Personal Simulation Graphics
FPGAdv Personal Pro      FPGAdv Personal Simulation Pro
```

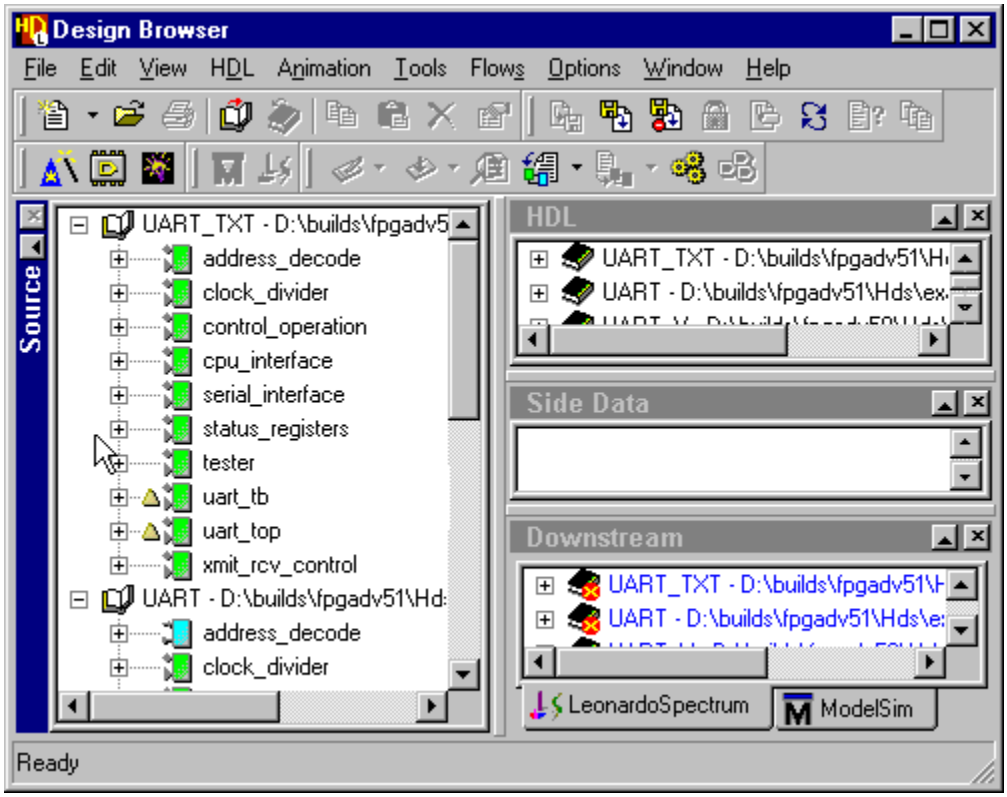
Please refer to the FPGA Advantage Start Here Guide to see more information about the above configurations.

You can invoke FPGA Advantage on UNIX using one of the following scripts if they are selected during installation:

```
<install_path>/Fpgadv/bin/fpgadvtxt (FPGA Advantage Text)
<install_path>/Fpgadv/bin/fpgadvgfx (FPGA Advantage Graphics)
<install_path>/Fpgadv/bin/fpgadvpro (FPGA Advantage Pro)
```

# Exploring the Designs

The HDL Designer Series (HDS) design browser will be displayed when the tool is invoked:




The design browser window is divided into four browsers:

- **Source** shows the graphical and textual source design data.
- **HDL** shows the generated code.
- **Side Data** displays an expandable indented list showing design and user data associated with the design unit view selected in the source browser.
- **Downstream** is a tabbed window which shows the data files prepared for ModelSim and LeonardoSpectrum.

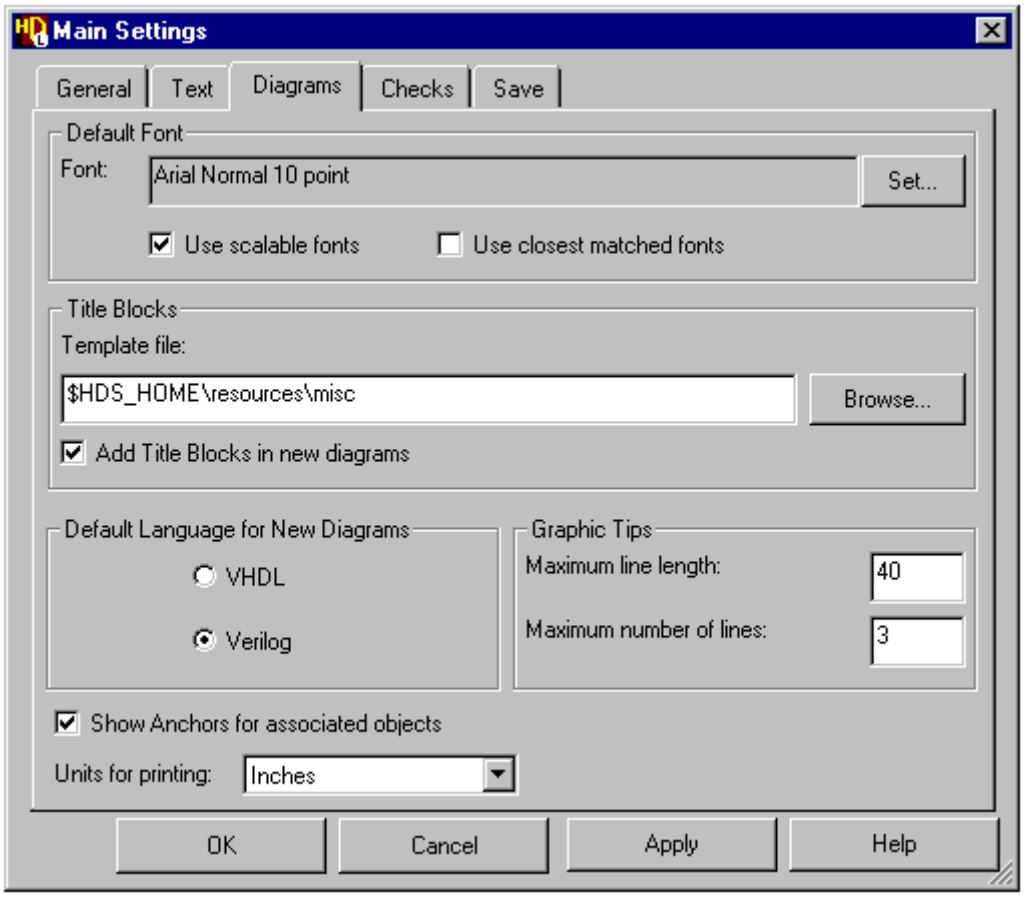
Three example libraries are displayed with their contents: a mixed language HDL text design named *UART_TXT*, a graphical VHDL design named *UART* and the corresponding graphical Verilog design named *UART_V*.

# Set Default Language

A set of default preferences are loaded when you invoke **FPGA Advantage** for the first time. There are separate tabbed dialog boxes for the main settings, VHDL and Verilog options, compile settings, HDL Import options, version management settings and master preferences for each type of graphical diagram. The preference dialog boxes can be accessed from the **Options** menu.

Choose **Main** from the **Options** menu to display the Main Settings dialog box, select the **Diagrams** tab and ensure that **Verilog** is set as the default language to be used for new diagrams. Use the OK button to confirm your language choice.

Choose VHDL if you would like to run this tutorial using the VHDL language.




All other preferences can be left with their default values for this tutorial.

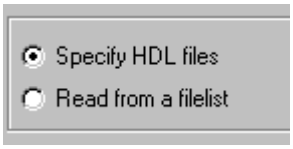
# Import the Fibonacci Design

This tutorial uses a design which is supplied as VHDL or Verilog code and can be imported using the HDL Import Wizard. This will recover any VHDL or Verilog code using HDL Import technology and convert it into HDS text views. You can display the imported design using the existing design browser.

From the **File** menu choose **Close All Libraries**. All browsers in the design browser should now be empty.

To import the Fibonacci Design, choose the pulldown  on the  button and select the  option from the palette (or choose **Text HDL Import** from the **HDL Import** cascade of the **HDL** menu).

Select **Specify HDL files** in the first page of the HDL Import wizard:




This tutorial can be completed using either the VHDL or Verilog example code depending upon your language preference. The language will be determined automatically providing that the source code file extension is recognized in the general preferences.

Click the **Next** button to display the **Specify HDL Source Files** page of the **HDL Import** Wizard.

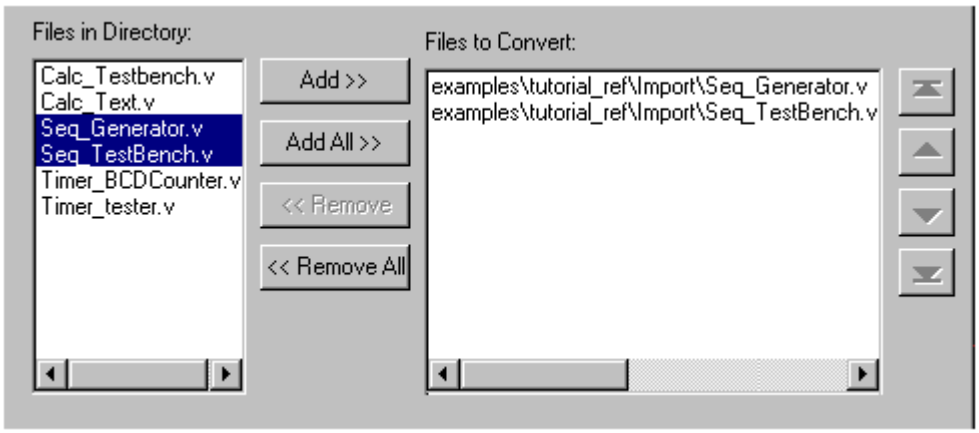
# Select Source HDL Files

Use the **Browse** button to locate the Fibonacci sequencer source code in the examples sub-directory of your FPGA Advantage installation as shown in the entry box below. For example, if FPGA Advantage has been installed in the directory D:\Builds\FPGAdvPersonal51, the pathname to locate all source HDL files would be:

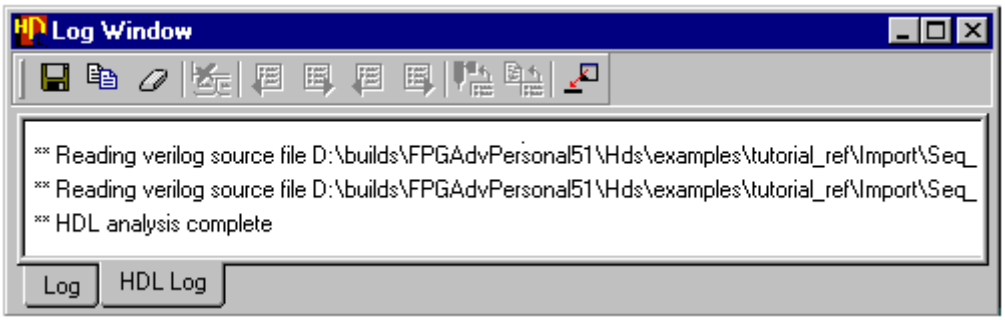
```
D:\Builds\FPGAdvPersonal51\Hds\examples\tutorial_ref\Import
```

Use the Files of type pulldown to select either VHDL or Verilog files. For example, Verilog files are shown selected below:


Select the *Seq_Generator* and the *Seq_TestBench* HDL files by using Ctrl + Left mouse button. Click Add >> to convert the files.

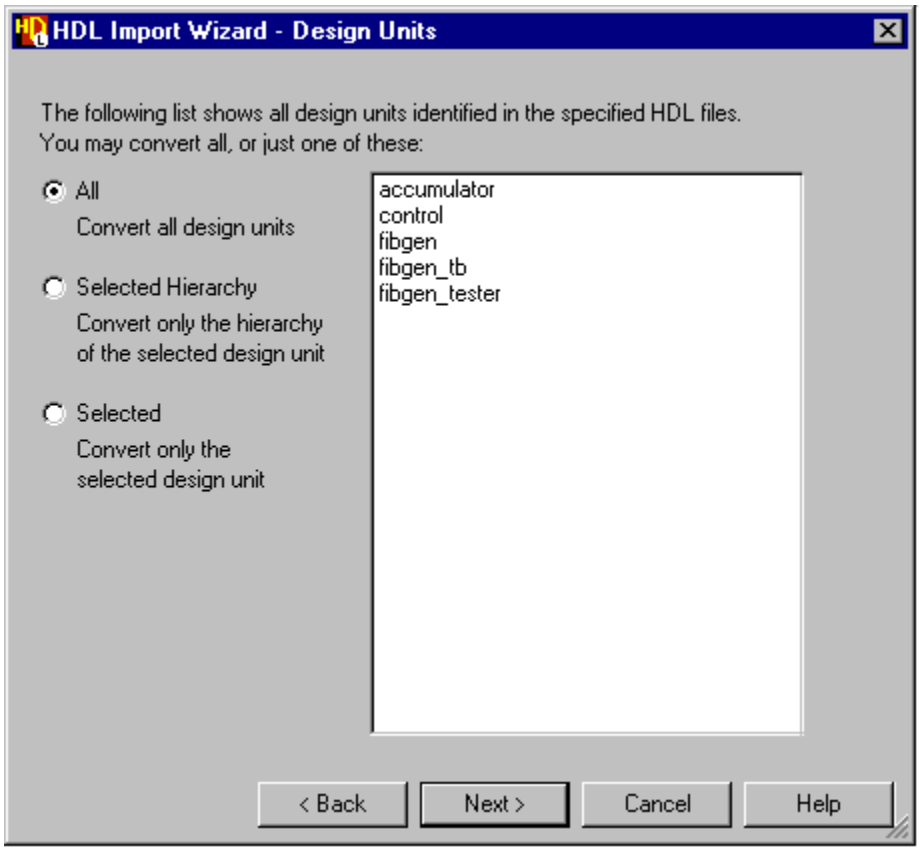


Click the **Next** button. You will now see the Log Window showing the Verilog source files for the Fibonacci design as they are read in:



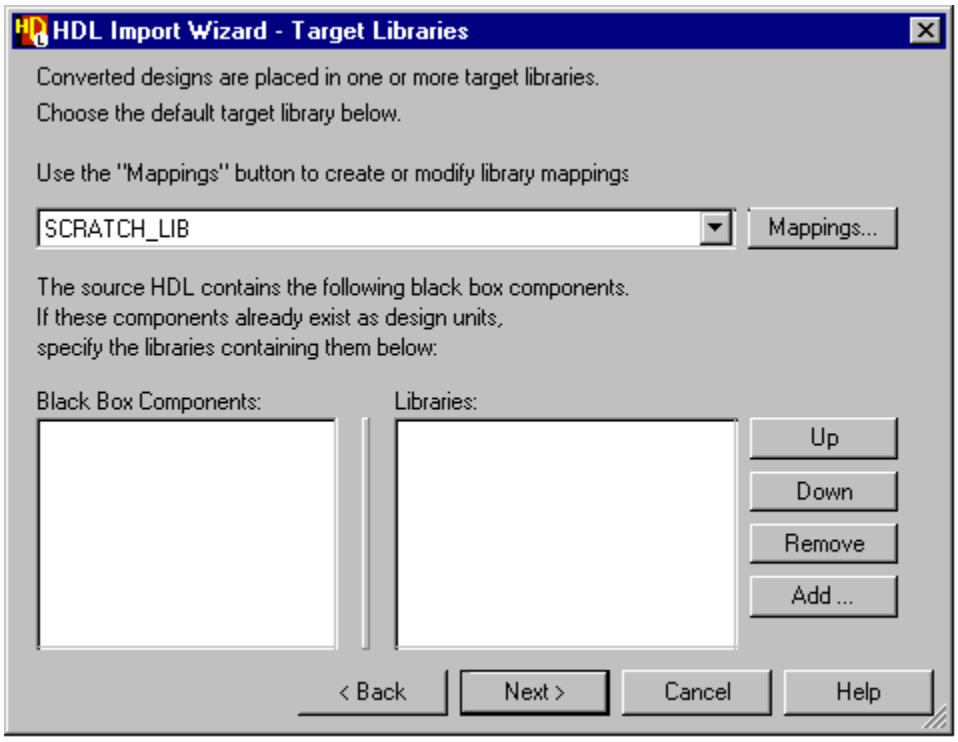

# Convert the Fibonacci Design

Each design unit now appears in a separate window in the HDL Import Wizard ready for conversion.

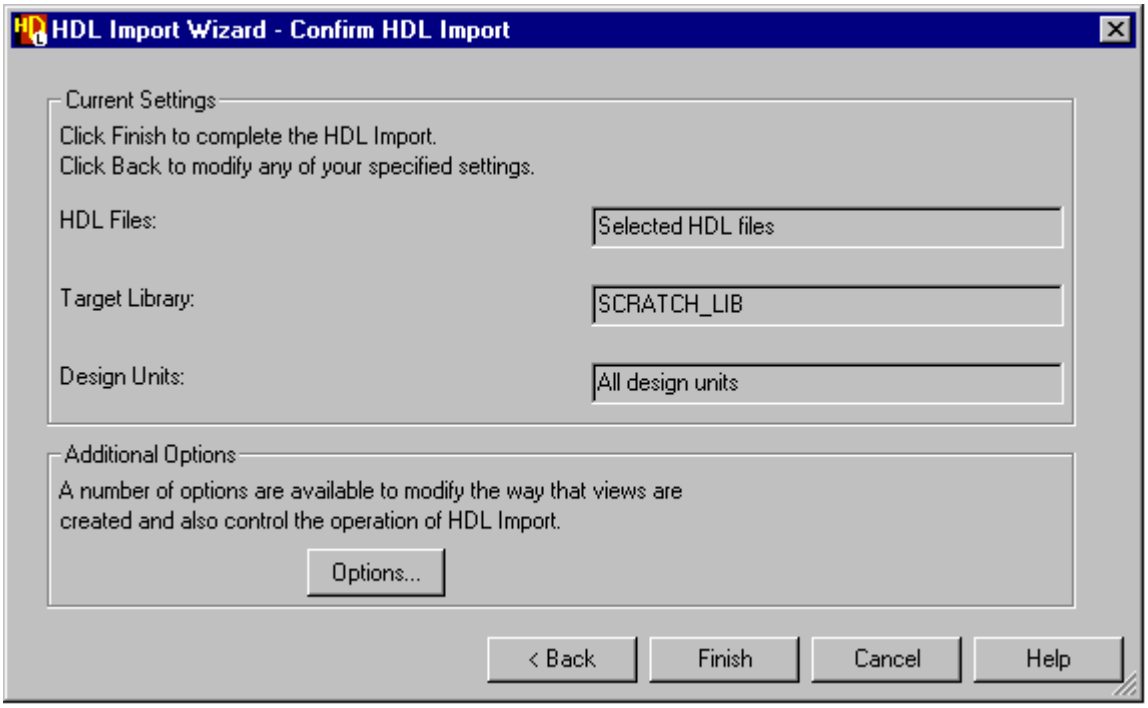



Click the **Next** button.

Select the SCRATCH_LIB library from the pulldown.




Click the **Next** button. The **Confirm HDL Import** dialog appears. Click the **Finish** button to convert the design.

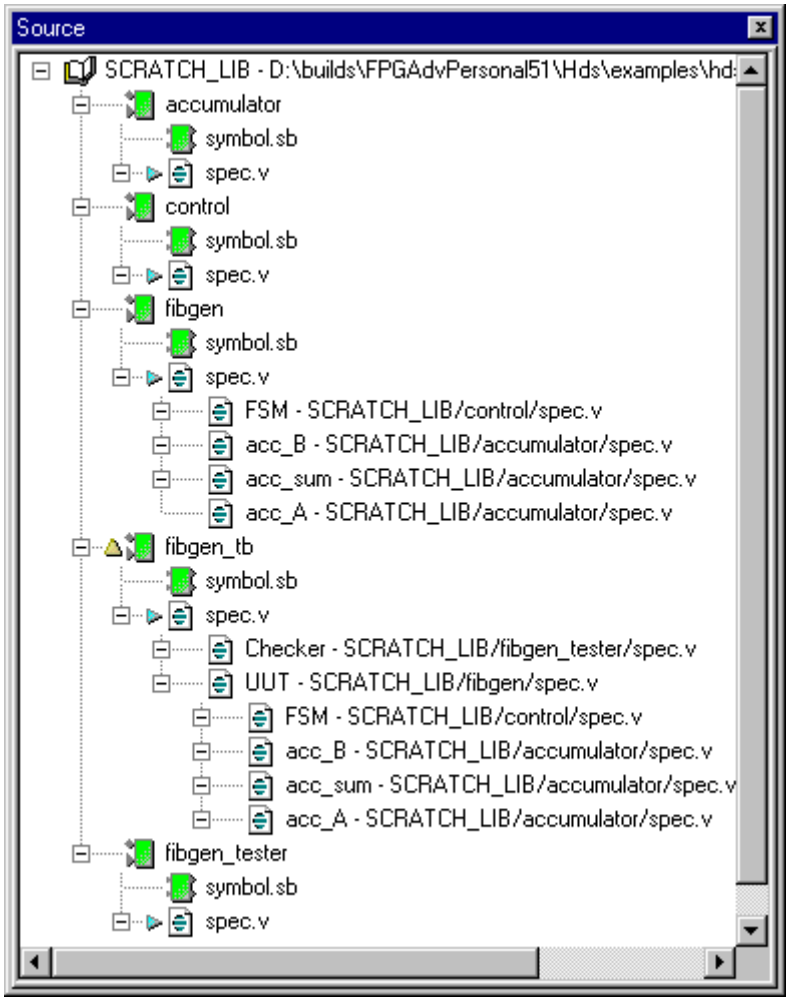


The HDL Log tab in the Log Window will indicate that a hierarchy of designs is being automatically created for the Fibonacci design and end with the following summary report:

```
1 top level design unit  [ fibgen_tb ]
5 HDS design units saved,
5 components
   5 HDL views
```

# Browsing the Fibonacci Design

Select the SCRATCH_LIB library in the source browser and choose **Expand All** from the popup menu. The design units for the Fibonacci design should now be displayed in the source browser as shown below:

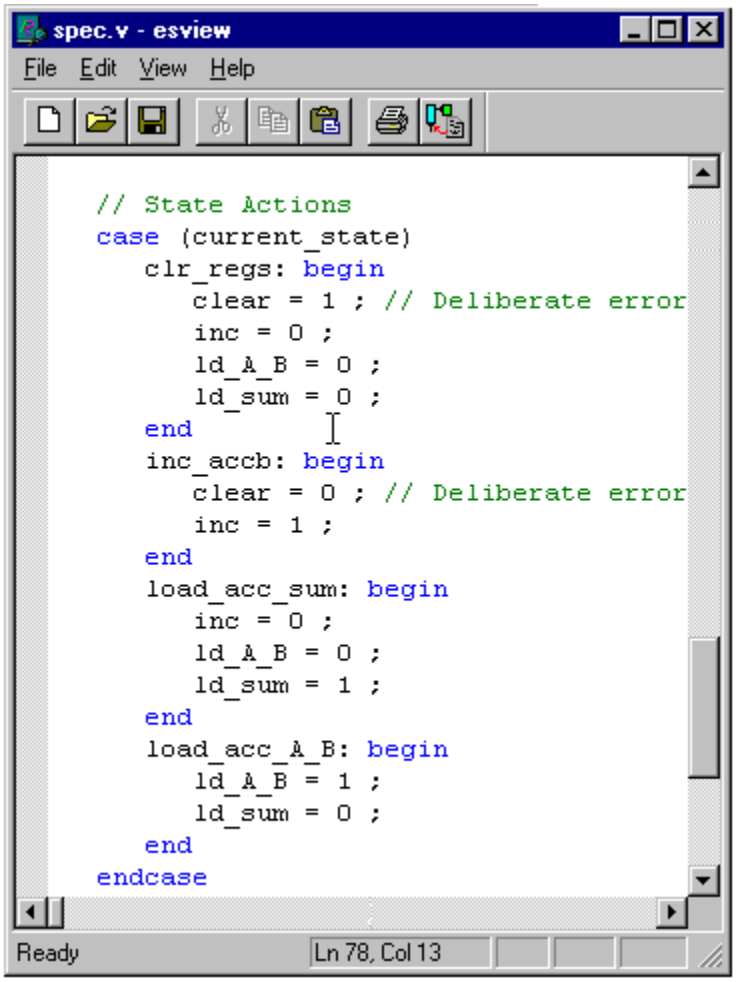



The Source, HDL, Side Data and Downstream browsers can each be undocked from the HDS design browser and viewed as a sub-window. This is achieved by holding down the left mouse button on the blue title bar and dragging the window completely away from the browser. Double clicking on the blue title bar when a browser is undocked will return the sub-window to the HDS design browser.

# Examine the State Machine Text View

Double-click on the icon representing the *control* component design unit in the HDS design browser to display the following state machine in text view.

Use the scroll bar to view the code and notice that there are two deliberate errors which have been added.




The Verilog version of the state machine is shown. The VHDL version will be similar.

Close the text editor.

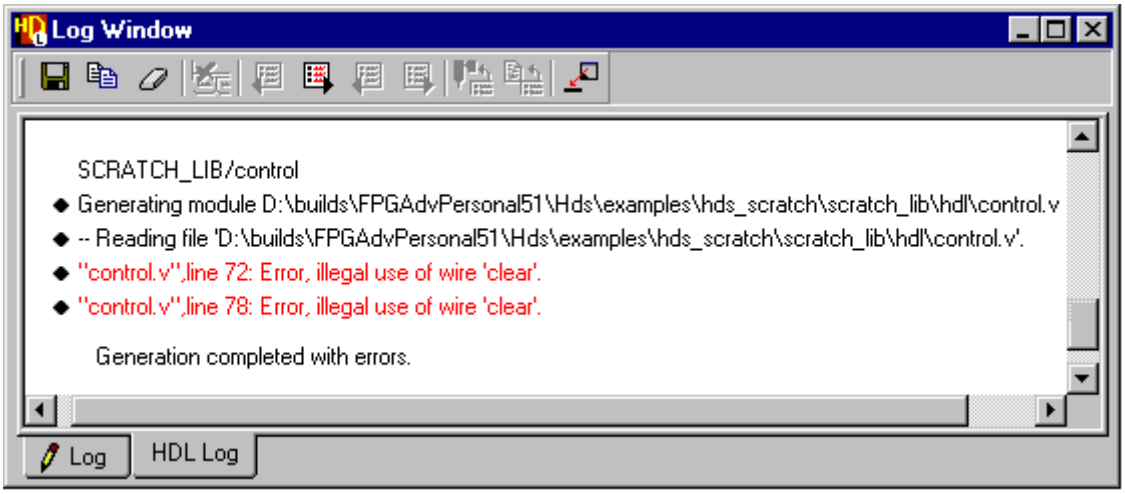
# Generate HDL for the State Machine

Select the component design unit icon for *fibgen_tb* which is displayed with a "top of design" marker in the HDS design browser.

Choose **Hierarchy Through Components** from the **Generate** cascade of the **HDL** menu in the design browser.

Notice that the Log Window now displays two error messages which have been deliberately added to the state machine text view.

The signal *clear* has been incorrectly entered and needs replacing with *clr*.

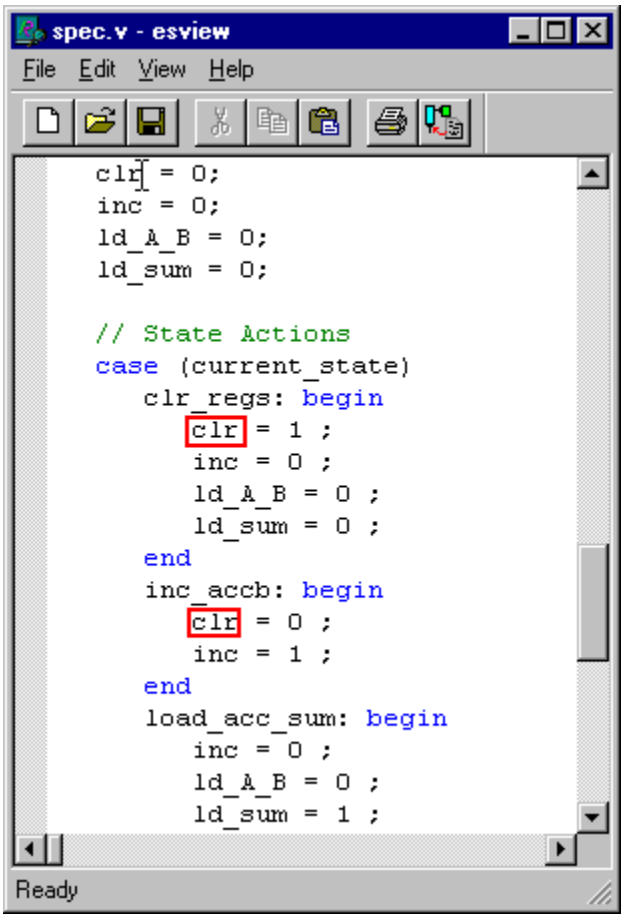


# Correct the State Machine Errors

Make the Log Window active and double-click on the line containing the error in the log window. You should now be able to edit the code using the ESView text editor which appears by default.

Replace *clear* with the word *clr* and delete all of the comment text after the semi-colon. Save your changes and close the editor.

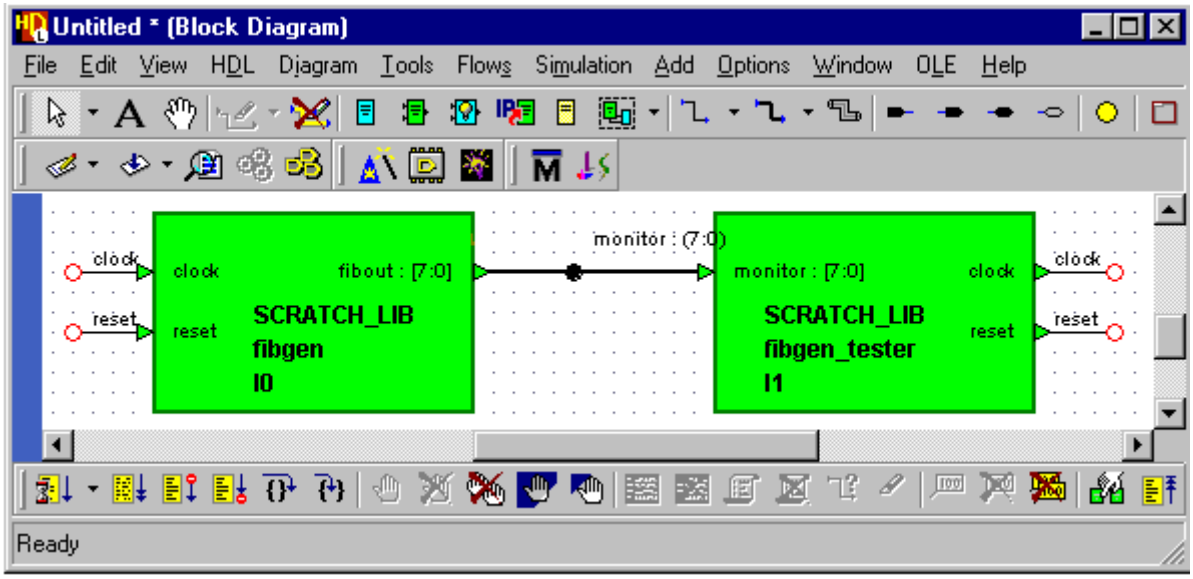
Repeat this procedure for the second occurrence of the error. The modified code should look similar to the example shown below.



# Create Graphical Test Bench

Choose **Block Diagram** from the **New** cascade of the **File** menu in the design browser.

Use the  button to display the Add Instance dialog box. Select the *SCRATCH_LIB* library and the *fibgen* component and click the OK button to add the *fibgen* component to the block diagram. Press the right mouse button and place the component on the diagram. Repeat the procedure and add the *fibgen_tester* component.




Position the mouse over the *fibgen* component and choose **Add Signal Stubs** from the popup menu. Two signals, *clock* and *reset* are added to the diagram plus a bus named *fibout.*

Repeat this procedure a second time for the *fibgen_tester* component. The WARNING messages which appear can be ignored. This is because the net *clock* and *reset* already exist and the port and net declarations differ. Click OK to acknowledge the warning message.

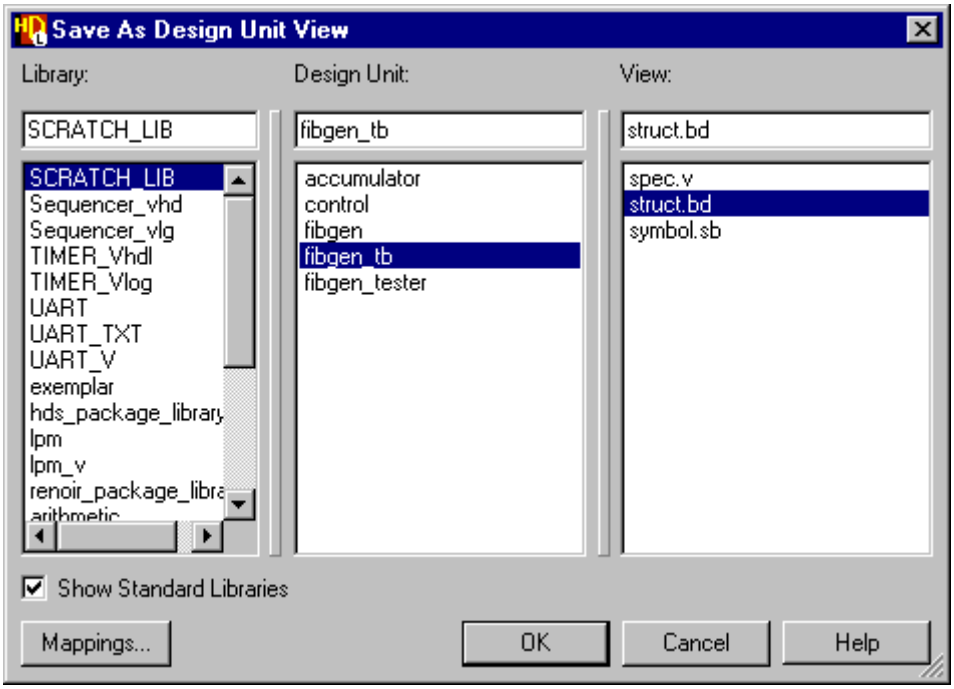
Note from the diagram that two further *clock* and *reset* signals have been added plus a second bus named *monitor*.

Select and delete the signal *fibout*. Drag and connect the signal *monitor* to the port *fibout.* The finished block diagram should look like the one shown above.

# Save the Test Bench

Use the button to save the test bench. The Save As Design Unit View dialog box is displayed which allows you to save a design unit into any currently mapped library. The columns allow you to specify the design unit name with its default view type.

Select the *SCRATCH-LIB* library and save the design unit name as *fibgen_tb*. The Save As dialog box should look similar to the example shown:




Click the OK button to save the test bench.

# Simulate Your Design

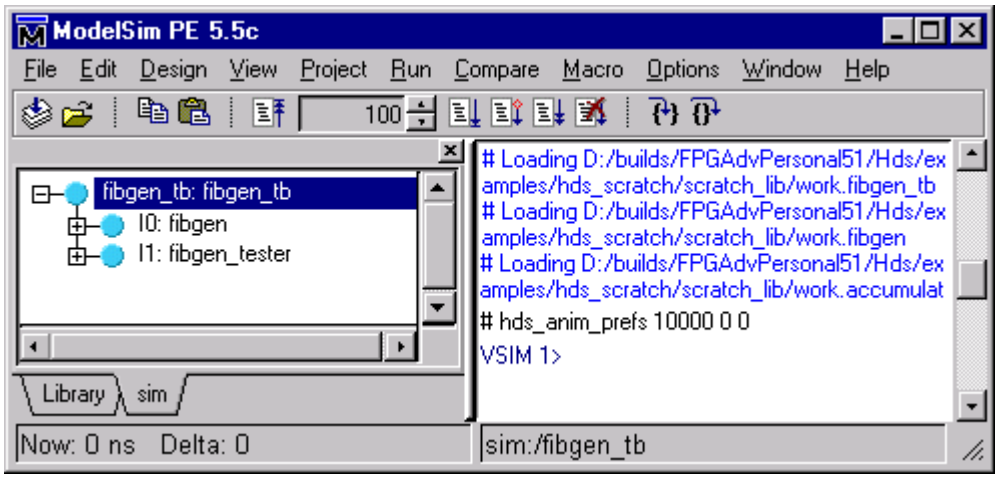
Select *struct.bd* view below *fibgen_tb* from the design browser and choose **Set Default View** from the popup menu. This will define the graphical test bench view *struct.bd* as the default view before simulating the design. Notice that the green triangle now appears next to *struct.bd* indicating the default view.

Select the *fibgen_tb* component and select the button from the toolbar. Messages will now appear in the HDS Log Window confirming that the HDL has been compiled for all the HDS design units.

Click the OK button to confirm the Start ModelSim dialog box.

This simulation flow button is set up to automatically generate and compile HDL for the hierarchy below the selected design unit. If generation and compilation are completed successfully, the ModelSim simulator is invoked and the entire compiled design is loaded.

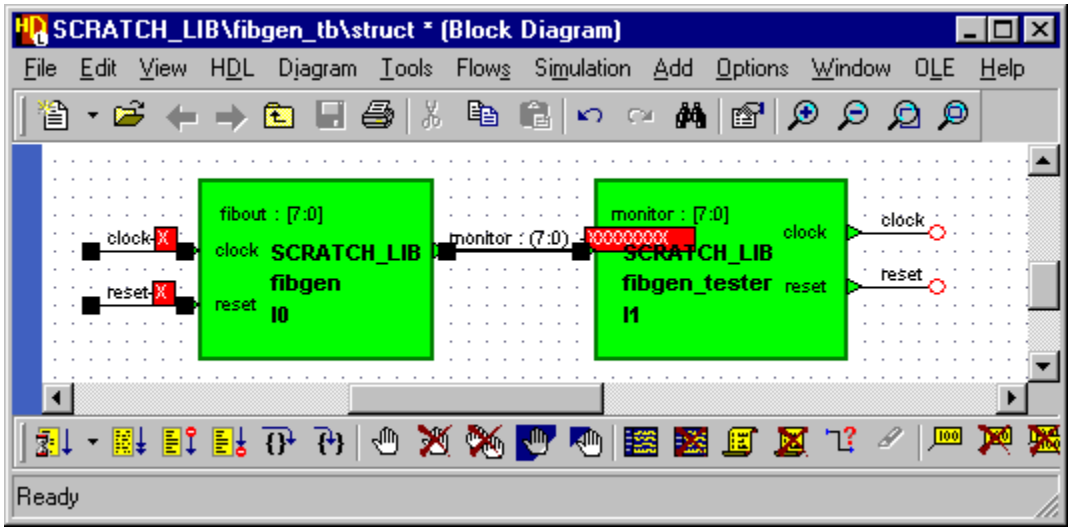
The progress of HDL generation and compilation are shown in the HDS Log Window. Notice that most design units are generated but all design units are compiled. If any compilation errors are detected when you compile a design, you can cross-reference from the HDS Log Window to the source graphics or generated HDL in the same way as for HDL generation errors.



# Add Probes to the Test Bench

Open the *fibgen_tb* block diagram from the HDS design browser. Use the view area button or zoom in until the diagram looks similar to the one shown below. You can select multiple signals by using Shift + Left mouse button or by dragging a box crossing the required signals.

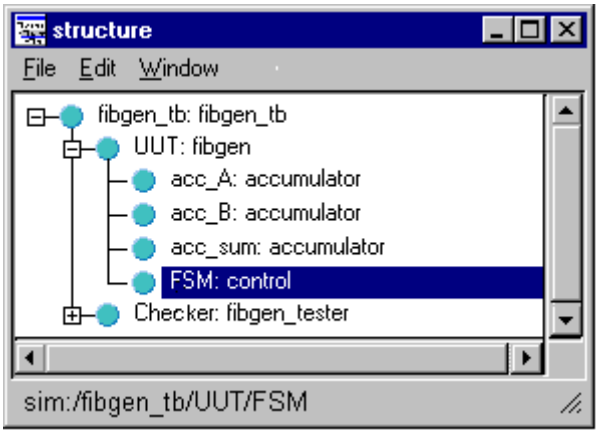
Select the three signals *monitor*, *clock* and *reset* as shown in the diagram.



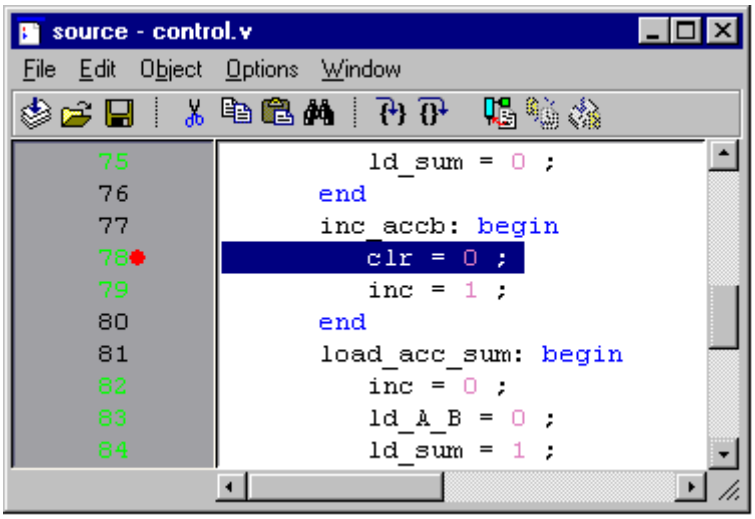

Notice that when the simulator is invoked there is an additional simulation toolbar displayed at the bottom of the HDS block diagram. Click the button to add simulation probes showing the current value of each signal.

# Add a Breakpoint

In the *fibgen_tb* block diagram view, choose **Structure** from the **View** cascade of the **Simulation** menu in the design browser. A window showing the fibgen_tb hierarchy will appear. Expand the hierarchy underneath fibgen tb and select the FSM: *control* view.



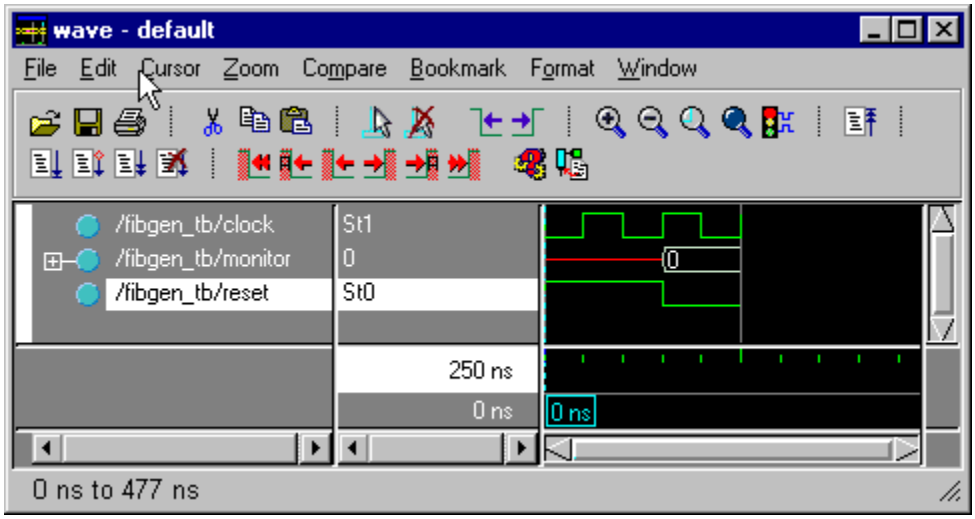

In the *fibgen_tb* block diagram view, choose **Source** from the **View** cascade of the **Simulation** menu. The state machine source window appears as shown below. Navigate to line 78 in the code by using the scroll bar and add a breakpoint by the side of the number by pressing the left mouse button. A red dot will be shown




indicating that a breakpoint is set.

# Run the Simulator

Make the *fibgen_tb* block diagram active and click the button to automatically open the ModelSim Wave window. Select the *fibgen_tb/monitor* signal as shown, and press the right mouse button and choose **Unsigned** for the **Radix** cascade of the popup menu.




In the *fibgen_tb* block diagram view click the to advance simulation by the default simulator timestep (100 nanoseconds). Notice that the signal values are initialized in the simulation probes on the test bench block diagram.

Click the button to run the simulator until the next breakpoint. Notice that the waveform appears as the simulation advances. Notice that an arrow appears next to the red dot in the *control.v* source window.

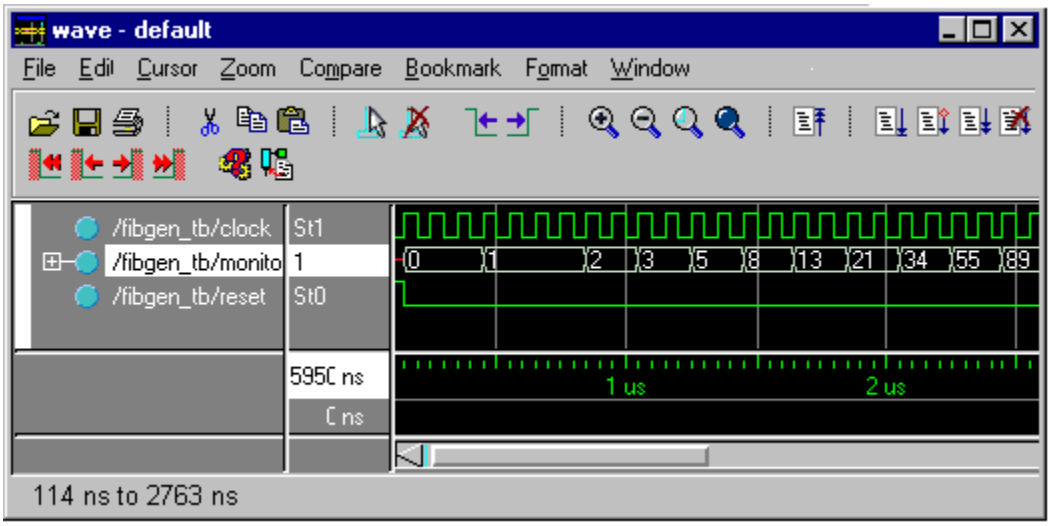
Finally, make sure that the state machine source window is active and remove the breakpoint. You can do this in the *control.v* source window. Pull down the **Edit** menu and select breakpoints. When the breakpoint dialog appears click on the **Delete All BP** button. Click the **Close** button and notice that the red dot disappears indicating that the breakpoint is unset.

# Complete the Simulation

Click the button adjacent to the button on the toolbar and select **Choose** from the popup menu. Another dialog will appear prompting you to enter a time interval to run the simulator. Enter 3000 into the entry box and click **OK** to run the simulator.


Alternatively, you can enter a time interval in the ModelSim window and then run the simulator.

Choose **Zoom Full** from the **Zoom** menu in the Wave window to display the full simulation waveforms which should look similar to the picture below for a successfully verified design.



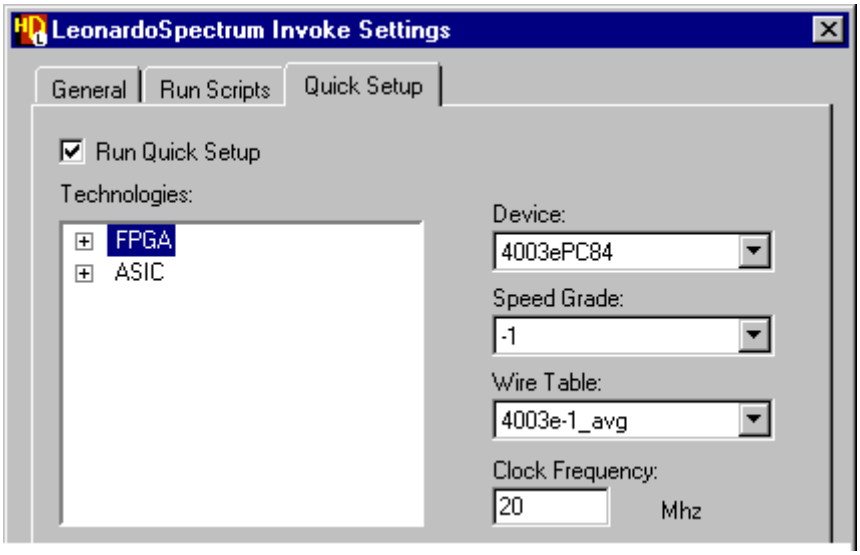

Simulation is now complete. Choose **Quit** from the ModelSim **File** menu to exit from the simulator. Click **Yes** to the exit message and close the HDS block diagram and state machine windows.

# Invoke LeonardoSpectrum

Select the *fibgen* component in the HDS design browser and then click on the  button. The LeonardoSpectrum Invoke Settings dialog is displayed.

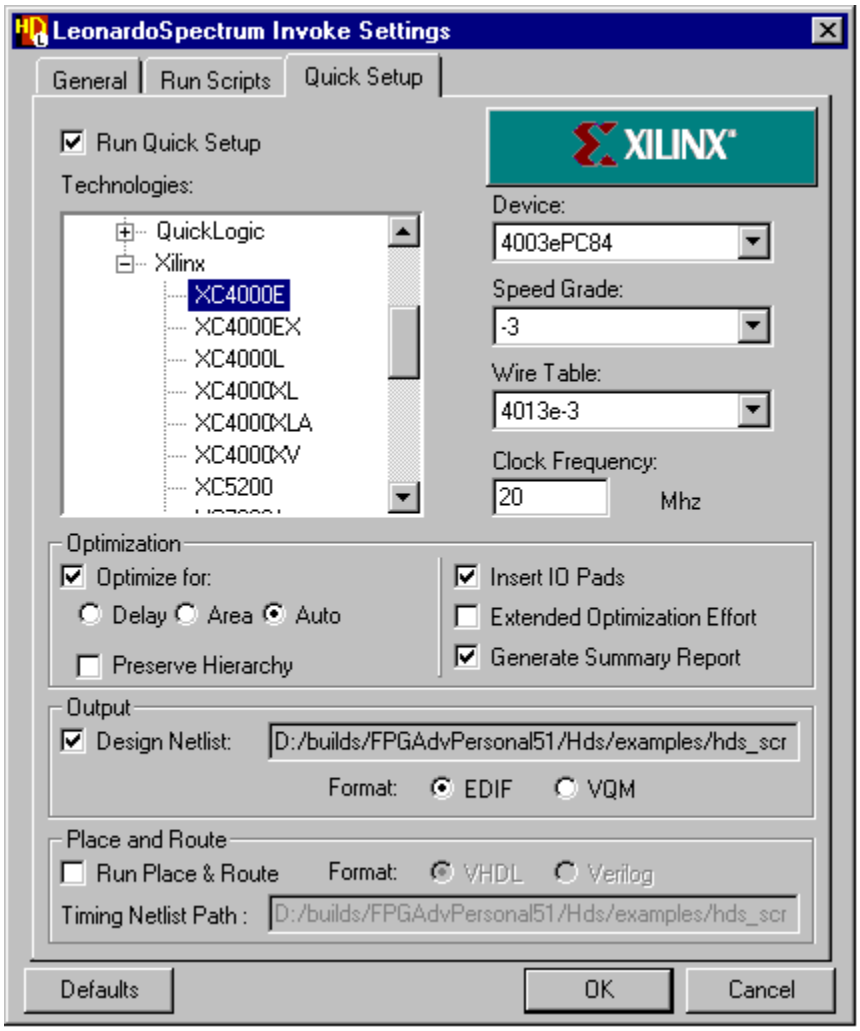
You cannot synthesize a test bench, so you must select the top level design unit for the actual design you want to synthesize.

Select the technology of your choice in the **Quick Setup** tab. For example, choose FPGA and Xilinx XC4000E by using the ⊞ buttons to expand the list of FPGA technologies available.




If you are using the *FPGA Advantage Personal* configuration with level 2 synthesis, ASIC libraries are not available and you can choose the Xilinx library directly.

When you select a technology, default values are automatically entered in the **Device, Speed Grade,** and **Wire Table** fields (these may vary from the ones shown below). The remaining fields will be set by default. Enter the value 20 in the **Clock Frequency** field and synthesize your design by clicking the **OK** button.

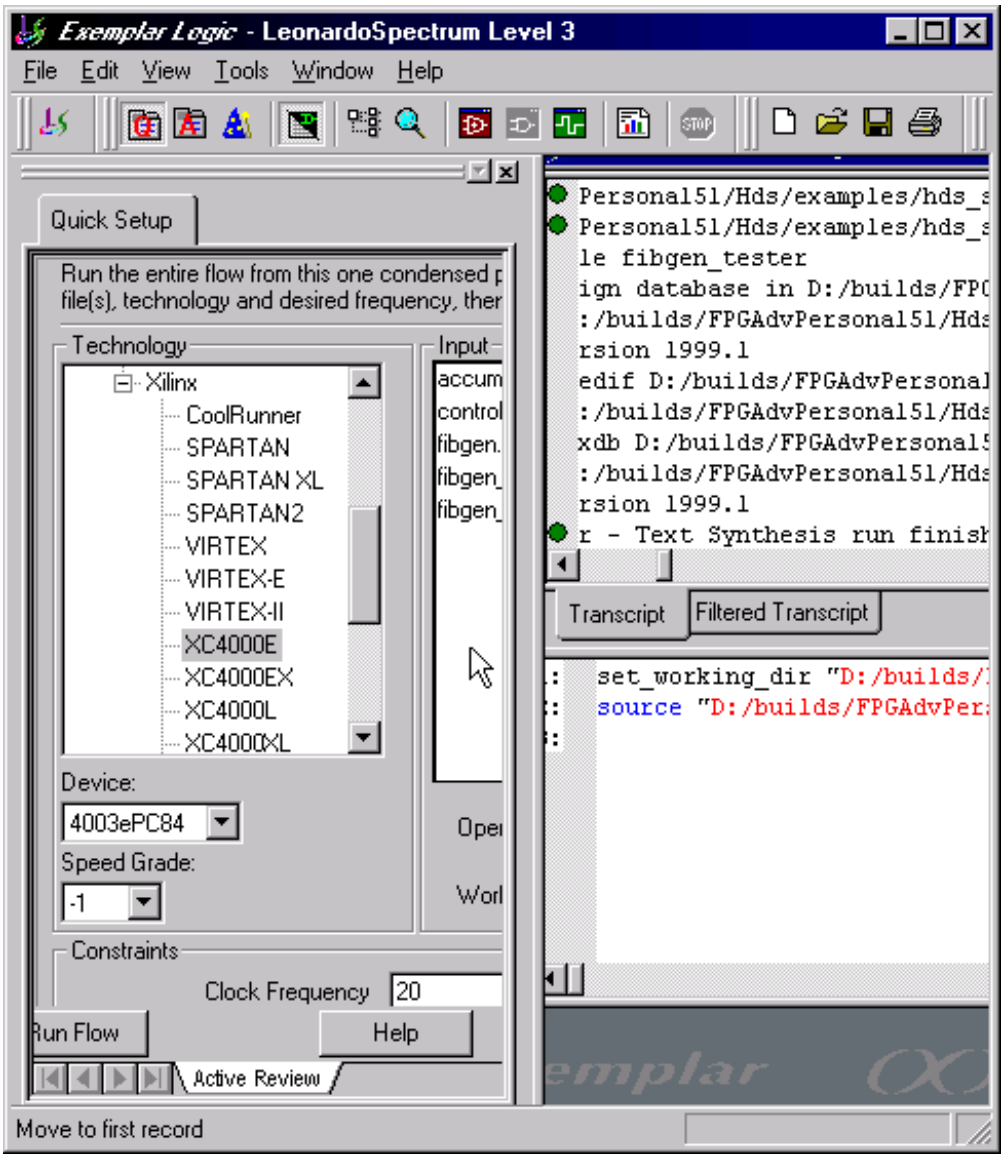



You are prompted to confirm the LeonardoSpectrum license.

You must choose a Level 2 license if you are using any of the *FPGA Advantage Personal* configurations. If you are using any of the *FPGA Advantage* configurations, select a Level 3 license. You can uncheck the **Run license selection next time** option if you want to run synthesis without prompting for the license level next time you invoke.

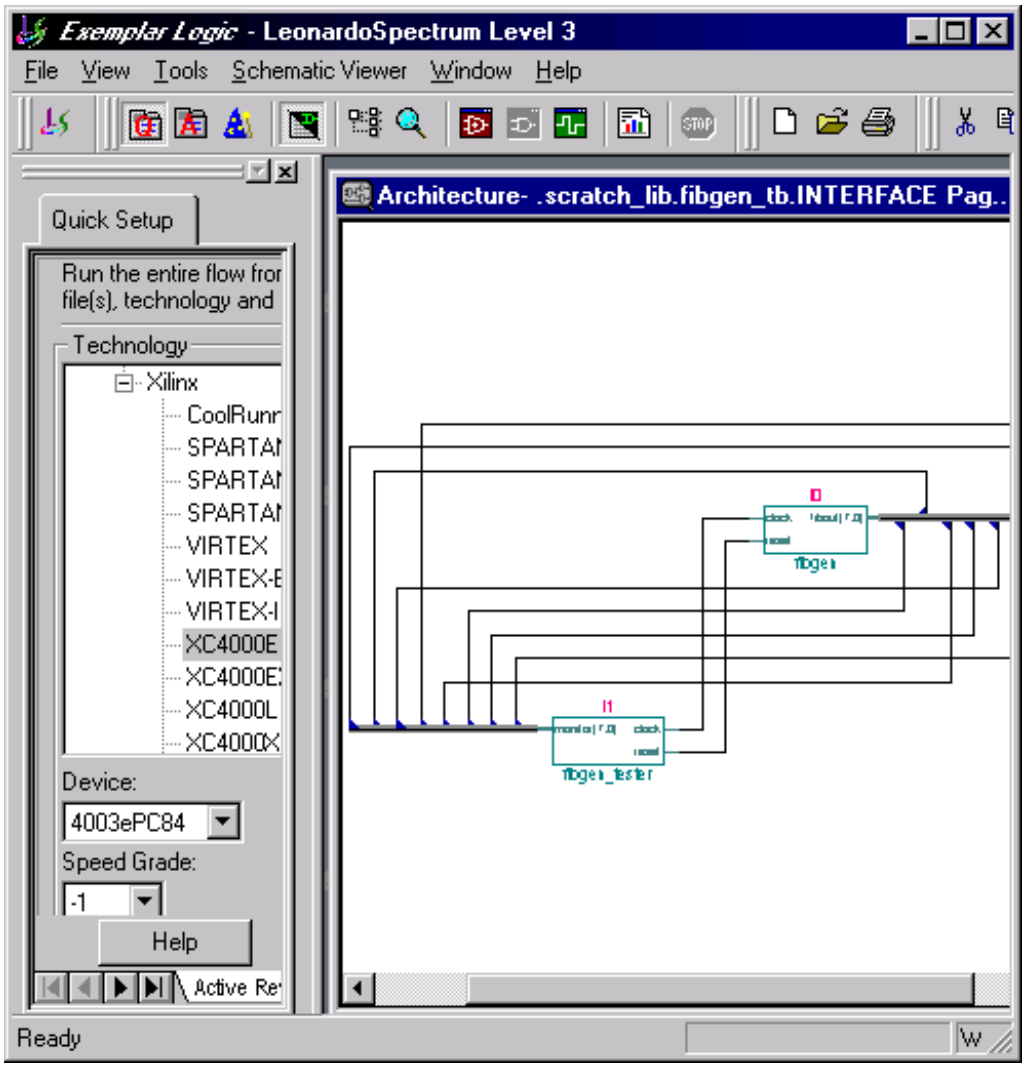
When you click the **OK** button LeonardoSpectrum is invoked on the entire design and the HDL files for your design are shown in the **Quick Setup** tab.

LeonardoSpectrum will optimize the design. Progress and completion messages will be displayed in the information window showing that the synthesis run has finished.



# View the RTL Schematic

If you are using the Level 3 license for LeonardoSpectrum, you can display an RTL Schematic for your design by clicking the button. You can move around the schematic using the scroll bars and the diagram can be enlarged inside the browser by choosing **Zoom In** from the **Zoom** cascade of the **Schematic Viewer** pulldown menu.




The Schematic Viewer is not available with a LeonardoSpectrum level 2 license. However, a license can be added if you obtain an additional license feature for LeonardoInsight.

You can cross-probe from the schematic to the corresponding object in a HDS source diagram. This is achieved by selecting an instance on the schematic and clicking the right mouse button. To view the HDS source diagram choose **Trace to HDL Designer** from the popup menu. The relevant HDS design unit view is displayed.

Close the text editor windows.

Exit from LeonardoSpectrum by choosing **Exit** from the LeonardoSpectrum **File** menu, choosing **No** from the confirmation dialog box.

Exit from HDS by choosing **Exit** from the **File** menu in the Design Browser window and choosing **Yes** from the confirmation dialog box.

# Further Information

You have now completed the FPGA Advantage *Getting Started Tutorial* and seen the complete design flow from importing HDL into HDS, through verification using the ModelSim simulator and used LeonardoSpectrum to synthesize a gate level netlist.

Each of these tools support a large range of features which cannot be illustrated in this simple tutorial. For more information, see the documentation which is available from the **Help** menu in each tool.

You can also access documentation from the **FPGA Advantage 5.1 > Bookcase** which can be opened on Windows from the **Programs** cascade of the **Start** menu. On UNIX, this document can be accessed by opening the Adobe Acrobat document *DocIndex.pdf* which can be found in the FPGA Advantage installation at: `<install_dir>/Doc/DocIndex.pdf.`

The **FPGA Advantage Bookcase** can also be accessed from the **Help** pulldown menu in the design browser on both Windows and UNIX by selecting **Help > FPGA Advantage Bookcase.**